

FIG. 2

PRIOR ART

FIG. 2

FIG. 2 is a block diagram of a memory system architecture. The system includes a READ, PROG, and ERASE control bus connected to a REFERENCE GENERATOR 257. The generator provides Vref, Vp1, Vp2, and Vp3 signals. An X-DECODE & BUS 263 receives address signals (Vp1, Vp2, Vp3) and outputs X0-n signals to a MEMORY BLOCK CELL ARRAY 67. A Y-DECODE & BUS 265 receives Y0-n signals and outputs Y0-n signals to the same array. A BIT LINE OR VIRTUAL GROUND SELECT 261 and a SENSE AMP 269 are also connected to the array. An output OUT is provided by the sense amp. A dashed box labeled 'PRIOR ART' encloses the array and select components.

FIG. 3: Detailed schematic of a memory cell array. The array consists of word lines (WL0, WL1, WL14, WL15) and bit lines (BL0, BL1, BL14, BL15). Memory cells are labeled MC0, MC1, MC14, and MC15. A dashed box labeled 'PRIOR ART' encloses the array. A table below the array defines the array mode and read bias for selected and unselected word lines, gate lines, and bit lines.

ARRAY MODE	READ BIAS
SELECTED WL	V ₀ (ground)
UNSELECTED WL	V ₀ , 20 (e.g., V ₀)
GSL	V ₀
GSL	V ₁ (e.g., 1.8 V)
BL OF PROGRAM CELL	V ₀
BL OF ERASE CELL	V ₁ = V ₀ + V ₀
V ₀ BLK	V ₀

PRIOR ART

FIG. 3

FIG. 3 is a detailed schematic of a memory cell array. The array consists of word lines (WL0, WL1, WL14, WL15) and bit lines (BL0, BL1, BL14, BL15). Memory cells are labeled MC0, MC1, MC14, and MC15. A dashed box labeled 'PRIOR ART' encloses the array. A table below the array defines the array mode and read bias for selected and unselected word lines, gate lines, and bit lines.

Document ID	Kind Codes	Source	Issue Date	
1	US 20040151050	US-PGPU	20040805	48
2	US 20040109344	US-PGPU	20040610	22
3	US 20040105310	US-PGPU	20040603	16
4	US 20040027907	US-PGPU	20040212	42
5	US 20020130341	US-PGPU	20020919	64
6	US 20020118018	US-PGPU	20020829	26
7	US 20020114191	US-PGPU	20020822	11
8	US 20020036942	US-PGPU	20020328	93
9	US 20020027818	US-PGPU	20020307	43
10	US 20020001245	US-PGPU	20020103	43
11	US 20010040834	US-PGPU	20011115	93
12	US 6750527 B1	USPAT	20040615	75
13	US 6574161 B2	USPAT	20030603	82
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FIG. 4

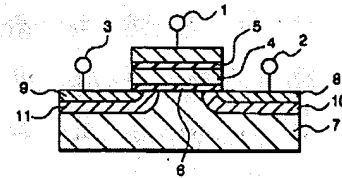


FIG. 5

